REMARKS

Applicant greatly appreciates the detailed examination evidenced by the Official Action mailed October 7, 2002 (hereinafter the Official Action). Applicant has amended several of the claims to further clarify the recitations of those claims in response to the Examiner's suggestions. For example, dependent Claims 36 and 39 have been amended as suggested by the Examiner. Claims 40 and 41 also have been amended herein to recite that the closed via/conductive pattern "penetrates **through** the dielectric layer" which is supported, for example, by Figure 2 of the application as filed. Applicant also has redrafted Claim 37 as new Claim 42 to further clarify the recitations of repeatedly and sequentially forming the steps recited in independent Claim 35.

However, with respect to the rejections of the independent claims, Applicant respectfully maintains that the claims are patentable over Sato. For example, Sato does not disclose **a dielectric layer having first and second opposing faces that includes a closed via therein that extends from the first face to the second face**. Applicant, therefore, maintains that the claims are in condition for allowance for at least the reasons discussed herein.

Amended Claims 40-41 comply with 35 USC § 112.

Claims 40-41 stand rejected under 35 USC § 112, first and second paragraphs. *Official Action, page 2.* Claims 40-41 have been amended to recite in-part:

> wherein the closed via penetrates **through** the dielectric layer and extends towards the integrated circuit substrate

The Official Action appears to argue that because some of the exact terminology from the claims is not recited in the specification, the claims do not comply with § 112, first paragraph. For example, the Official Action states that the subject matter of "penetrates" is not defined by the originally filed specification. *Official Action, page 2.* Applicant respectfully points out that under MPEP § 2163, the standard for evaluating compliance with § 112, first paragraph, is whether Applicants' disclosure, as of its filing, conveys **with reasonable clarity** that which is claimed. Moreover, the MPEP specifically points out that

the subject matter of the claim need **not be described literally** in the specification. MPEP § 2163.02.

As shown in Figure 2 of the application as filed, in some embodiments according to the present invention, the portions of the conductive layer pattern 50a, labeled S2, penetrate through interdielectric layer pattern 48b and extend toward the substrate 40. Accordingly, Applicant respectfully submits that Claims 40-41 comply with 35 USC § 112, and, therefore, request that the rejections thereto be withdrawn.

Claims 36, 37 and 39-41 comply with 35 USC § 112

Claims 36, 37 and 39-41 stand rejected under 35 USC § 112. *Official Action, page 2.* With respect to the rejection of Claims 36 and 39, Applicant has amended these claims to further clarify the relationships between the dielectric layers and conductive patterns recited therein as suggested by the Examiner. Accordingly, amended Claims 36 and 39 comply with 35 USC § 112, second paragraph, and the rejections thereto are respectfully requested to be withdrawn.

With respect to the rejection of Claim 37, Applicant has cancelled this claim and has added new Claim 42 to further clarify the patentable subject matter recited therein. In particular, new Claim 42 recites in part:

> forming a second dielectric layer having first and second opposing faces on the first conductive pattern, the second dielectric layer including a closed via therein that extends from the first face of the second dielectric layer to the second face of the dielectric layer and that encloses an inner portion of the second dielectric layer, and is enclosed by an outer portion of the second dielectric layer; and then
>
> forming a second conductive pattern on the second dielectric layer that extends from the first face of the second dielectric layer to the second face of the second dielectric layer in the closed via and on the second dielectric layer opposite the substrate to form a multilayer bonding pad on the integrated circuit substrate.

As demonstrated by the above-cited portions of Claim 42, a second dielectric layer is formed on the first conductive pattern followed by forming a second conductive pattern on the second dielectric layer. Accordingly, Applicant submits that new dependent Claim 42

complies with 35 USC § 112, second paragraph and respectfully requests that the rejections thereto to be withdrawn.

As discussed above, Claim 40 has been amended to recite in-part:

> forming a dielectric layer having first and second opposing faces on an integrated circuit substrate, the dielectric layer including a closed via therein that extends from the first face to the second face and that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer, wherein the closed via **penetrates through the dielectric layer** and extends towards the integrated circuit substrate; and
>
> forming a conductive pattern that extends from the first face to the second face in the closed via and on the dielectric layer opposite the substrate.

Dependent Claim 41 has been similarly amended. Accordingly, the amended recitations of Claims 40 and 41 further clarify that the conductive pattern **penetrates through** the dielectric layer. For example, in some embodiments according to the present invention as illustrated in Figure 2 of the application, portions S2 of the conductive pattern 50a penetrate through the dielectric layer 48b and extend toward the substrate 40. Amended Claims 40 and 41 comply with 35 USC § 112, second paragraph. The Applicant therefore respectfully requests the withdrawal of the rejections.

If, however, the Examiner still maintains the rejection of these claims as outlined above, Applicant invites the Examiner to suggest a term other than "penetrates through" that the Examiner would find acceptable while accurately describing the material discussed above.

Independent Claim 35 is patentable over Sato

Claims 35-41 stand rejected under 35 USC § 102 over U.S. Patent No. 5,739,587 to Sato ("Sato"). *Official Action, page 5.* Applicant respectfully traverses the rejection of the claims as Applicant maintains that the independent claims are patentable over Sato, as Sato does not disclose, for example:

> forming a dielectric layer **having first and second opposing faces** on an integrated circuit substrate, the dielectric layer including a closed via therein **that extends from the first face to the second face** and that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer; and

forming a conductive pattern that extends from the first face to the second face in the closed via and on the dielectric layer opposite the substrate.

Independent Claim 35 and 40.

Anticipation under § 102 requires that each and every element of the claim is found in a single prior art reference. *W. L. Gore & Associates Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983). Stated another way, all material elements of a claim must be found in one prior art source. *In re Marshall*, 198 U.S.P.Q. 344 (C.C.P.A 1978). "Anticipation under 35 U.S.C. § 102 requires the disclosure in a single piece of prior art of each and every limitation of a claimed invention." *Apple Computer Inc. v. Articulate Systems Inc.* 57 USPQ2d 1057, 1061 (Fed. Cir. 2000). A finding of anticipation further requires that there must be no difference between the claimed invention and the disclosure of the cited reference as viewed by one of ordinary skill in the art. *See Scripps Clinic & Research Foundation v. Genentech Inc.*, 927 F.2d 1565, 1576, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991). Additionally, the cited prior art reference must be enabling, thereby placing the allegedly disclosed matter in the possession of the public. *In re Brown*, 329 F.2d 1006, 1011, 141 U.S.P.Q. 245, 249 (C.C.P.A. 1964). Thus, the prior art reference must adequately describe the claimed invention so that a person of ordinary skill in the art could make and use the invention.

As understood by Applicant, the Official Action relies on Figures 1, 3 and 8 of Sato (along with associated passages of Sato) for the rejection of independent Claims 35 and 40. In an effort to further clarify Applicant's reasoning and to advance prosecution of the present application, Applicant provides herein a detailed analysis of Figures 3, 8 and 11 and the associated passages of Sato cited by the Official Action.

As understood by Applicant, Figure 3 of Sato illustrates an interlayer insulation film 60 having a plurality of interlayer connection conductors 40-45. The interlayer connection conductors 40-45 appear to have the same structure as that of conductor 120 shown in Figures 1 and 2 of Sato (see, for example, the passage in Sato relating to the diameters of the interlayer connection conductors). *Sato, column 5, lines 5-8.*

In contrast to Figure 3 of Sato, independent Claims 35 and 40 recite, in-part, "forming a dielectric layer . . . including a closed via therein . . . that encloses an inner portion of the

dielectric layer and is enclosed by an outer portion of the dielectric layer." As illustrated by Figures 1, 2 and 3 of Sato, the conductors that pass through the dielectric layer, appear to be solid, cylindrical structures that do not enclose **any** portion of the interlayer insulation film 60 (alleged to disclose the dielectric layer recited in the claims). Accordingly, Figures 1-3 of Sato do not disclose all of the recitations of independent Claim 35 as required under section 102.

As understood by Applicant, Figure 8 of Sato is a plan view of an upper electrode layer 100 including a center through-hole. Furthermore, Figure 8 illustrates concentric structures 102 and 103 around the center through-hole in the upper electrode layer 100. The conductors 102 and 103 shown in Figure 8 are **grooves** in the upper electrode layer, and do not appear to pass through the upper electrode layer into what would be an interlayer insulation film (as illustrated, for example, in Figure 3 of Sato). For example, the relevant portion of Sato states that

> As shown in FIG. 8, furthermore, **grooves may be formed in concentric circles around a through hole. Conductors 102, 103 and 104 may be embedded into the grooves and through hole.** The double-groove layout can reliably prevent the moisture from entering the semiconductor device. *Sato, col. 6, lines 36 to40.*

As understood by Applicant, a groove does not disclose a hole. The above-cited passage of Sato demonstrates that Figure 8 illustrates a through hole (having a conductor 104) in the upper electrode layer 100 and concentric grooves that have conductors 102 and 103 embedded therein.

Moreover, even assuming for the sake of argument that the conductors 102 and 103 shown in Figure 8 did pass through the upper electrode layer 100, such a structure would still not disclose all the recitations of independent Claims 35 and 40. In particular, independent Claims 35 and 40 recite in-part that the closed via (included in the dielectric layer) "extends from the first face to the second face" (of the dielectric layer). In contrast to Figure 8 of Sato, in some embodiments according to the present invention as illustrated, for example, in Figure 2 of the application, the interdielectric layer pattern 48b has first and second opposing faces (bordering, for example, layers 46a and 50a, respectfully). The interdielectric layer pattern 48b includes a closed via which is illustrated in the cross-section of Figure 2 by the sections

labeled as S2. In the plan view of Figure 1, the areas S2 are shown as being part of a closed via 54 that encloses an inner portion of the interdielectric layer pattern 48b and is enclosed by an outer portion of the interdielectric layer pattern 48a. Furthermore, the closed via in the interdielectric layer pattern 48b (as illustrated by portions as S2 in Figure 2) extends from the first face of the interdielectric layer pattern 48b to the second face of the interdielectric layer pattern 48b. Accordingly, Figure 8 of Sato also does not disclose the recitations of independent Claim 35 as required under section 102.

As understood by Applicant, Figure 11 of Sato illustrates a structure (similar to the structure shown in Figure 3) but with an additional interlayer insulation film 540 having holes therein and conductors 611 that pass through the holes to contact a bottom electrode layer 550. *See, for example, Sato, column 7, lines 1-11.* Sato, therefore, appears to add only another layer of the same structure shown in Figure 3 of Sato which, as discussed above, also does not disclose the recitations of independent Claims 35 and 40. Accordingly, Figure 11 also does not disclose all of the recitations of independent Claim 35 as required under section 102.

Independent Claims 35 and 40 are patentable over Sato for at least the reasons discussed herein. Furthermore, dependent Claims 36, 38-39, 41, and 42 are patentable at least per the patentability of the independent claims.

Many of the dependent Claims are separately patentable over Sato.

As discussed above, Claims 36, 38-39, 41, and 42 are patentable at least per the patentability of the independent claims. In addition to the reasons discussed above in reference to the independent claims, many of the dependent claims provide separate bases for patentability of Sato. For example, Sato does not disclose that "the closed via is at least one of a circular, elliptical, and polygonal via" as recited in dependent Claim 38." Contrary to assertions in the Official Action, Figures 3, 8, and 11 do not disclose these recitations.

As recited in independent Claims 35 and 40, the via "encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer." Therefore, according to dependent Claim 38, the (circular, elliptical, polygonal) via recited in independent claim 35 encloses an inner portion of the dielectric layer, and is enclosed by an

outer portion of the dielectric layer. As discussed above in reference to independent Claim 35, Figure 8 of Sato shows concentric conductors 102-104 in grooves **in an electrode layer**. Therefore, as understood by Applicant, the concentric conductors 102-104 in Figure 8 of Sato do not enclose an inner portion of the **dielectric layer**, and are not enclosed by an outer portion of **the dielectric layer**. Figures 3 and 11 of Sato also do not disclose these recitations. Accordingly, Claim 38 is patentable over Sato for at least these additional reasons.

CONCLUSION

Applicant has amended Claims 36, 39, 40 and 41 to further clarify the patentable subject matter recited therein. Applicant has shown that the claims comply with 35 USC § 112. Applicant also has shown that independent Claims 35 and 40 are patentable over Sato for at least the reasons discussed herein. Accordingly, Applicant respectfully requests the withdrawal of all rejections and the allowance of all claims in due course. If any informal matters arise, the Examiner is encouraged to contact the undersigned by telephone at (919) 854-1400.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: BOX NON-FEE AMENDMENT, Commissioner for Patents, Washington, DC 20231, on January 7, 2003.

Audra Wooten
Date of Signature: January 7, 2003

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Sir:

The following is an addendum to the concurrently filed amendment in response to an Official Action dated October 7, 2002 in the above referenced application. This addendum includes a marked-up version of the changes made to the claims by the present amendment.

In the Claims:

Claim 36 has been amended as follows:

36. (Twice Amended) A method according to Claim 35 wherein the step of forming the conductive pattern comprises the step of forming [a] the conductive pattern filling the closed via and on the dielectric layer opposite the substrate.

Claim 37 has been canceled without prejudice or disclaimer.

Claims 39 - 41 have been amended as follows:

39. (Twice Amended) A method according to Claim 35:

wherein the step of forming the dielectric layer comprises the step of forming [a] the dielectric layer on an integrated circuit substrate, the dielectric layer including the closed via and an open via therein; and

wherein the step of forming the conductive pattern comprises the step of forming [a] the conductive pattern in the closed via, in the open via and on the dielectric layer opposite the substrate.

40. (Twice Amended) A method of forming a bonding pad for an integrated circuit comprising the steps of:

forming a dielectric layer having first and second opposing faces on an integrated circuit substrate, the dielectric layer including a closed via therein that extends from the first face to the second face and that encloses an inner portion of the dielectric layer, and is enclosed by an outer portion of the dielectric layer, wherein the closed via penetrates through the dielectric layer and extends towards the integrated circuit substrate; and

forming a conductive pattern that extends from the first face to the second face in the closed via and on the dielectric layer opposite the substrate.

41. (Amended) A method according to Claim 40 wherein the step of forming the conductive pattern comprises forming the conductive pattern in the closed via and on the dielectric layer opposite the substrate, wherein the conductive pattern penetrates through the dielectric layer and extends towards the integrated circuit substrate.

Claim 42 has been added as follows:

42. (New) A method according to Claim 35 wherein the dielectric layer comprises a first dielectric layer and the conductive pattern comprises a first conductive pattern and the closed via comprises a first closed via, the method further comprising:

forming a second dielectric layer having first and second opposing faces on the first conductive pattern, the second dielectric layer including a second closed via therein that extends from the first face of the second dielectric layer to the second face of the dielectric layer and that encloses an inner portion of the second dielectric layer, and is enclosed by an outer portion of the second dielectric layer; and then

forming a second conductive pattern on the second dielectric layer that extends from the first face of the second dielectric layer to the second face of the second dielectric layer in the second closed via and on the second dielectric layer opposite the substrate to form a multilayer bonding pad on the integrated circuit substrate.

END